REMARKS

Present Status of the Application

Claims 1-5 and 7-16 are pending, of which claims 1 and 7 have been amended in order to more explicitly describe the claimed invention, and claims 15-16 have been canceled. It is believed that no new matter adds by way of amendments made to claims or otherwise to the application. For at least the foregoing reason, Applicants respectfully submit that remaining claims 1-5 and 7-14 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion of the claim rejection under 35 USC 103

1. The Office Action rejected claims 1, 5, 7, 11-13 and 15-16 under 35 USC 103(a) as being unpatentable over Lach et al.(US-6,108,212, hereinafter Lach) in view of Sakai et al. (US-5,894,984, hereinafter Sakai).

Applicants respectfully disagree and traverse the above rejections as follows. Applicants provide an improved substrate structure of Flip Chip package having higher reliability. Applicants recognized that, because there is no clearance between the bump and the solder mask layer after the bump is attached to the bump pad for the SMD design, the SMD design is relatively hard to generate voids, thus the product yield can be improved in the subsequent under-filling process. However, the collapse phenomenon and the bondability between the bump and the mounting pad are poor in the SMD design and, therefore, the demand for the coplanarity of the substrate of the flip chip package is relatively rigorously required, and the process tolerance is relatively small. Further, Applicants also recognized that in an NSMD design there is a clearance between the bump and the pad opening, the contact area is relatively large as it includes the ones on the top and side surfaces. Therefore, the collapse phenomenon is relatively good, and the bondability is relatively robust. Thus the tolerance for the coplanar error of the substrate of the flip chip package is relatively large. However, in order to avoid the generation of the void in the subsequent under-filling process, the pad opening of the solder mask layer needs to be enlarged properly. As a result, the pitch of the mounting pads needs to be increased to meet this requirement, thus the packaging density becomes lower, and this

makes the layout work of the substrate of the flip chip package relatively difficult. In light of the above, Applicants have designed the bonding pads of a substrate structure of Flip Chip package that combines the advantages of both the SMD and the NSMD design. In accordance with the above objects, the present inventors proposes a substrate structure of Flip Chip package comprising at least "a solder mask layer covering the patterned circuit layer on the surface of the substrate of the flip chip package, the solder mask layer partially covering a first top surface of the first mounting pads by being in direct contact with entire sidewalls and a portion of the top surface of the first mounting pads while entirely exposing a second top surface and sidewalls of the second mounting pads, wherein the first mounting pads are disposed at a peripheral region of the substrate and the second mounting pads are disposed at a central region of the substrate", as recited in the amended claims 1 and 7.

The advantages of the above arrangement of SMD and NSMD mounting pads structure are:

firstly, since the top surface and the sidewalls of the second mounting pads that are disposed in the central region are completely exposed, the clearance space between the second mounting pads in the central region is relatively large and, therefore, the coplanar tolerance is also relatively large;

secondly, since the first mounting pads that are disposed in the peripheral region are essentially a SMD structure, the bumps (254) corresponding to the first mounting pads (214) can only be attached to the top surface (214a) of the first mounting pads 214. Because there is no clearance between the bumps and the solder mask, there no underfill materials is required to fill this (peripheral) area and, thus, no voids are formed in this region. Further, since the central region 220 is relatively spacious, and the pitch of the second bonding pads 216 is relatively large, i.e., the pad opening is relatively large, the underfill material can fill this space without the risk of forming voids. Therefore, the yield can be effectively promoted; and

thirdly, because the bumps (254) attach not only the top surface (216a) but also the side surfaces 216b of the second bonding pads, the collapse phenomenon can be relatively insignificant. Therefore, the quality of bump-to-mounting pad attachment is

promoted.

Accordingly, Applicants provides a substrate structure for a flip-chip package by very cleverly making use of different types of mounting pad structure within the flip-chip package in a manner to produce a novel substrate structure that has higher tolerance of the coplanar error and at the same the process yield can also be effectively promoted.

To the contrary, Lach substantially teaches a surface-mount device package comprising a pad located on a face of the surface-mount device, a solder bump bonded to the pad, and a terminal spaced radially apart from the pad. A terminal surrounds the pad in at least one common plane that bisects the pad and the terminal. An electrically resistive volume intervenes between the pad and the terminal. The pad is electrically coupled to the terminal through the resistive volume. The terminal, the pad, and the electrically resistive volume cooperate to form a passive component associated with at least one device interconnection. The passive component preferable comprises an integral resistor. The integral resistor serves to eliminate or at least substantially reduce electrical resonances and reflections that may otherwise degrade the signal integrity. It is clear that Lach does not teach, suggest or disclose any structure or method for improving the tolerance coplanar error as taught by the present inventors much less teaching the arrangement of SMD and NSMD mounting pads for achieving higher tolerance of coplanar error or promoting the filling of the underfill material for achieving higher process yield.

More specifically, Lach does not teach or suggest a *solder mask layer partially covering a first top surface of the first mounting pads by being in direct contact with entire sidewalls and a portion of the top surface of the first mounting pads.* As shown in Figs. 1 and 2 of Lach, the solder mask layer 40 only covers a portion of the top surface of the bonding pad 27 and is not in contact with the entire sidewalls of bonding pad 27. In fact, Lach teaches against contacting the sidewalls of bonding pad 27 with the solder mask layer 42 because "[A]n electrically resistive volume 36 intervenes between the pad 27 and the terminal 34. The pad is electrically and resistively connected to the terminal 34 through the resistive volume 36. The terminal 34, the component pad 27, and the electrically resistive volume 36 cooperate to form an integral resistor 32". Col. 3, lines

33-38 and Fig. 2.

The Office Action also acknowledged that Lach does not depict the layout of the mounting pads, wherein the first mounting pads surround all of the second mounting which are located in the central region of the substrate, however, pointed out that Sakai teach in FIG. 6a, a layout of mounting pads, wherein the first mounting pads 8b surround the second mounting pads 8a which are located at a central region of the substrate. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a layout of mounting pads in Lach device, wherein the first mounting pads surround all of the second mounting pads which are located at a central region of the substrate as taught by Sakai in order to reduce the short circuits in the device by preventing the formation of bridges across adjacent pads. The combination is motivated by Sakai who point out the advantages of using mounting pads layout as depicted in FIG. 6a (col. 2, lines 13-53).

Applicants respectfully disagree. Sakai teaches an improved structure of an electronic part comprising a board, a circuit element disposed on the board having electrodes, a solder bumps disposed on the board each connected to one of the electrodes of the circuit element, and a substrate having disposed thereon electrodes each connected to one of the solder bumps. The electrodes of the substrate include a first group and a second group arranged around the first group. The electrodes of the first group have contact surfaces contacting with the solder bumps which are greater in area than contact surfaces of the electrodes of the second group.

However, Sakai does not teach or suggest one group pads are covered on their top surface and sidewalls by a solder mask layer while the other group pads are entirely exposed by the solder mask layer as required by claims 1 and 7. In other words, Sakai neither teaches a SMD structure nor a NSMD structure. The only difference between the two group pads of Sakai is the size or area of the top contact surface. The present invention is not about placing an arbitrary group of pads in the central region of a substrate and placing another group of pads at the peripheral region surrounding the first group. The present invention as defined in claims 1 and 7 requires that the group of pads in the peripheral region have a SMD structure, i.e., partially covered by the solder mask

layer, while the group of pads in the central region have a NSMD structure, i.e., totally exposed by the solder mask layer. Sakai is totally silent about the SMD and NSMD structure of pads much less teaching on the specific arrangement of the SMD and NSMD structure. Accordingly, Sakai cannot possibly teach, suggest or disclose the arrangement of SMD and NSMD mounting pads and, therefore, cannot cure the deficiencies of Lach in this regard. Therefore, no combination of Lach and Sakai can achieve or otherwise render the claimed invention obvious.

For at least the above reasons, claims 1 and 7 are patentable over Lach and Sakai. For at least the same reasons, their dependent claims 5, and 11-13 are also patentable over Lach and Sakai. Reconsideration and withdrawal of these rejections is respectfully requested.

2. The Office Action rejected claims 2-4, 8-10 and 14 under 35 USC 103(a) as being unpatentable over Lach and Sakai as applied to claims 1 and 7 above, and in further view of the APA.

Applicants respectfully submit that APA cannot cure the specific deficiencies of Lach and Sakai discussed above. Therefore, claims 1 and 7 are patentable over Lach, Sakai, and the APA. Claims 2-4, 8-10 and 14 depend from claims 1 and 7 and, thus, are also patentable over the cited art for at least the same reasons as set forth above.

Furthermore, these dependent claims contain features that further distinguish over the cited prior art. For example, claim 14 specifies that the bumps attach to both the top surface and side surfaces of the second mounting pads. Sakai clearly teaches away from claim 14. In Figs. 5(a)-5(c), the pads 8a in the central region are larger than the surrounding pads 8b. When connected, the central four of the bumps 6 to be connected to pads 8a spread in substantially a trapezoid form over upper surfaces of the central electrodes 8a *without being expanded laterally.* Col. 6, lines 41-43. In Figs. 7(a)-7(c), a through hole 14 is formed to accommodate a portion of the bumps 6 so that no bumps 6 attach to the sidewalls of the electrode. This illustrates that the proposed combination of Sakai with Lach against claim 14 is improper.

Reconsideration is respectfully requested.

3. The Office Action rejected claims 4 and 10 under 35 USC 103(a) as being unpatentable over Lach, Sakai and the APA as above, and further in view of Katchmar et al. (US-6,194,782, hereinafter Katchmar).

Applicants respectfully submit that still Katchmar cannot cure the specific deficiencies of Lach, Sakai and APA as discussed above and, therefore, claims 4 and 10 are patentable over the cited prior art for the same reasons as set foth above. Reconsideration is respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-5 and 7-14 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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